

In The Claims

1. (Original) A method for fabricating a device on a substrate, comprising:
forming a gate over said substrate;
forming a source/drain extension region in said substrate on each side of said gate,
said source/drain extension regions including dopants of a first conductivity type;
forming at least one corner diffusion region in said substrate, said corner diffusion region including dopants of a second conductivity type that is opposite to said first conductivity type and overlapping with at least a portion of one of said source/drain extension regions; and
forming source and drain diffusion regions in said substrate adjacent said source/drain extension regions on opposite sides of said gate, said source and drain diffusion regions being further away from said gate than said source/drain extension regions and including dopants of said first conductivity type.
2. (Original) The method of claim 1 wherein said source/drain extension regions extend between two opposite sides of said device and said corner diffusion region overlaps with a portion of a source/drain extension region near one of said opposite sides of said device.
3. (Original) The method of claim 1 wherein said source/drain extension regions extend between two opposite sides of said device and said corner diffusion region also extends between said two opposite sides of said device.
4. (Original) The method of claim 1 wherein said device occupies an active area of said substrate, and wherein forming corner diffusion regions comprises applying a mask on said substrate that exposes at least a portion of said active area near said gate.
5. (Original) The method of claim 4 wherein said active area is bordered on some or all sides by isolation regions in said substrate, said exposed portion of said active area being near at least one of said isolation regions.
6. (Original) The method of claim 1 wherein said device is fabricated on said substrate together with a plurality of other devices and wherein said corner diffusion regions

are formed during a sequence of processes for forming source/drain extensions in some of said plurality of other devices.

7. (Original) The method of claim 1, wherein said device is a PMOSFET device, wherein said source/drain extensions are formed using a PLDD implant process, and wherein said corner diffusion regions are formed using a NLDD implant process.

8. (Original) The method of claim 1, wherein said device is a NMOSFET device, wherein said source/drain extensions are formed using a NLDD implant process, and wherein said corner diffusion regions are formed using a PLDD implant process.

9-16 (Cancelled).

17. (Original) A method for fabricating an integrated circuit including NMOSFET and PMOSFET devices, comprising:

forming N-type diffusion regions in said NMOSFET devices; and
forming in at least some of said NMOSFET devices P-type diffusion regions simultaneously with at least one P-type diffusion region in at least one of said PMOSFET devices.

18. (Original) The method of claim 17 wherein said P-type diffusion regions in at least some of said NMOSFET devices and said at least one P-type diffusion region in at least one of said PMOSFET devices is formed using a PLDD implant process.

19. (Original) The method of claim 17, further comprising forming in at least some of said PMOSFET devices N-type diffusion regions simultaneously with at least one N-type diffusion region in at least one of said NMOSFET devices.

20. (Original) The method of claim 17 wherein said N-type diffusion regions in at least some of said PMOSFET devices and said at least one N-type diffusion region in at least one of said NMOSFET devices is formed using a NLDD implant process.

21-22 (Cancelled).